

### REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on August 26, 2003, and the references cited therewith. Claims 23, 24, 29, 32, 35, 39, and 43 are amended, claim 22 is canceled, and no claims are added; as a result, claims 21 and 23-45 remain pending in this application.

The amendment filed December 2, 2002 was objected to under 35 USC § 132. The objection stated that the amendment introduced new matter into the disclosure.

The objection in the present Office Action objects to inclusion of matter relating to a DRAM memory. Applicant submits that no reference to a DRAM memory has ever been introduced in the present divisional application. Applicant respectfully submits that this portion of the objection is therefore moot.

Applicant respectfully traverses remaining new matter objections and respectfully submits that no new matter was added. Applicant respectfully submits that use of embodiments of Applicant's invention in a memory device are discussed and supported on page 1, lines 8-16. Applicant further submits that one of ordinary skill in the art will recognize that a memory device includes an array of memory cells.

### §112 Rejection of the Claims

Claims 21-45 were rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The rejections state that, "There is nothing in the original disclosure relating to dynamic random access memory (DRAM) or to an array of memory cells." Applicant reiterates that no reference to a DRAM memory has ever been introduced in the present divisional application. Applicant respectfully submits that this portion of the rejection is therefore moot.

Applicant respectfully traverses the remaining rejections and submits that use of embodiments of Applicant's invention in a memory device are discussed and supported on page 1, lines 8-16. Applicant further submits that one of ordinary skill in the art will recognize that a memory device includes an array of memory cells.

Regarding claims 44 and 45, Applicant respectfully submits that limitations included in these claims are not method limitations. For example, an apparatus, such as a transistor or a switch can be manufactured with physical characteristics such that in a normal state is open or closed. Further, Applicant submits that method limitations in an apparatus claim are in fact proper as product-by-process claims pursuant to MPEP 2113.

The rejection further states that, “In order to be a voltage regulator a device has to sense a voltage level at a point where the voltage is to be regulated and control the voltage at that point.” Applicant respectfully submits that the level of detail needed for one of ordinary skill in the art to make and use the invention is disclosed in the present specification. For example, in the absence of additional details regarding a sensing operation, Applicant respectfully submits that upon reading the specification, one of ordinary skill in the art will understand how to implement a sensing operation in embodiments of the present invention.

Reconsideration and withdrawal of the 35 USC § 112, first paragraph rejections is respectfully requested.

Claims 21-45 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

The rejection states that, “It is still not clear how the voltage regulator is coupled to the substrate.” Applicant respectfully submits that “coupling” is definite under 35 USC § 112, second paragraph. Pursuant to MPEP § 2173.04, Applicant notes that “breadth of a claim is not to be equated with indefiniteness.” Examples of coupling elements of a voltage regulator include, but are not limited to, utilizing MOS fabrication techniques to form elements such as transistors or diodes as described in the specification. In further example, a source/drain region of a MOS transistor formed by ion implantation is coupled to a substrate.

Reconsideration and withdrawal of the 35 USC § 112, second paragraph rejections is respectfully requested.

§103 Rejection of the Claims

Claims 21-45 were rejected under 35 USC § 103(a) as being unpatentable over McLaury in view Bynum et al, Uchida and Sawamura.

The rejection states that, “McLaury shows apparatus for regulating substrate bias.”

McLaury appears to show a diode series 10. The reference also appears to show a diode load element 110. Embodiments of McLaury also appear to show a sense element as part of the integrated circuit. However, Applicant is unable to find at least one **bypass transistor** to at least one diode in a series of diodes for electrically bypassing at least one diode. In contrast, Applicant’s independent claims all include at least one bypass transistor to at least one diode in a series of diodes for electrically bypassing at least one diode.

The rejection states that, “Bynum et al shows the concept of controlling the bias applied to a substrate by shunting a diode in a line that applies a voltage to a substrate.” Bynum appear to show an integrated circuit designed to bias an epitaxial well. Embodiments of Bynum appear to include a single diode 42. Bynum also appears to show a shunt path in embodiments using the diode. However, Applicant is unable to find at least one **bypass transistor selectively controlled by a user**, the bypass transistor being coupled to at least one diode in the series of diodes for electrically bypassing at least one diode. Applicant respectfully submits that a shunt is not selectively controlled by a user. In contrast, Applicant’s independent claims, as amended, all include at least bypass transistor selectively controlled by a user, the bypass transistor being coupled to at least one diode in the series of diodes for electrically bypassing at least one diode.

The rejection states that, “Uchida shows a regulated power supply for an integrated circuit wherein switches shunt diodes in series to establish a desired voltage.” Uchida appears to show n diodes 123 connected in series to provide a fixed voltage. Uchida also appears to discuss an embodiment wherein a parallel circuit is set in a high impedance state at an initial stage and selectively set at a low impedance state at a programming stage. However, Uchida does not show a **bypass transistor selectively controlled by a user**, the bypass transistor being coupled to at least one diode in the series of diodes for electrically bypassing at least one diode. In contrast, Applicant’s independent claims, as amended, all include at least bypass transistor selectively controlled by a user, the bypass transistor being coupled to at least one diode in the series of diodes for electrically bypassing at least one diode.

Applicant is unable to find any reference to “switches” or “FETs” or “bipolar elements” as hypothesized by the Examiner. Because these elements do not appear to be from the Uchida reference, it appears that the Examiner is taking official notice of these elements. Applicant respectfully traverses this official notice and requests the Examiner to provide a reference that describes such elements. Absent a reference, it appears that the Examiner is using personal knowledge, so the Examiner is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

Further, Applicant respectfully submits that there is no teaching in Uchida or McLaury or Bynum to combine the references as suggested in the present Office Action. For example, Uchida deals with a power supply. There is no motivation to use teachings of Uchida to bias a substrate. The Office Action must provide specific, objective evidence of record for a finding of a suggestion or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *In re Sang Su Lee*, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002). The Office Action stated “it would have been obvious to one of ordinary skill in the art at the time of the invention to have adapted the controlling elements of Bynum et al or Uchida to the apparatus of McLaury,” which is a mere conclusory statement of subjective belief, so Applicant respectfully submits that the Office Action has not provided objective evidence for a suggestion or motivation to combine the references.

Applicant respectfully submits that Sawamura does not cure the deficiencies of the references discussed above.

Because the references do no show motivation to combine, the 35 USC § 103(a) rejection is not supported. Even if combined, because the cited references do not show every element of Applicant’s independent claims, a 35 USC § 103(a) rejection is not supported by the references. Reconsideration and withdrawal of the rejection is respectfully requested with respect to Applicant’s independent claims 21, 24, 29, 32, 35, 39, and 43. Additionally, reconsideration and withdrawal of the rejection is respectfully requested with respect to the remaining claims that depend therefrom as depending on allowable base claims.

Regarding claims 44 and 45, Applicant respectfully submits that limitations included in these claims are not method limitations. For example, an apparatus, such as a transistor or a switch can be manufactured with physical characteristics such that in a normal state is open or closed.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 373-6944) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

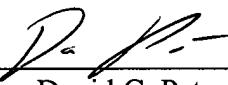
Respectfully submitted,

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Date 11-20-03

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 20th day of November, 2003.

Name

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Signature

